Bihar Engineering University, Patna

End Semester Examination - 2022

Course: B.Tech. | *Semester: III* | *Time: 03 Hours*

Code: 100305 | *Subject: Digital Electronics* | *Full Marks: 70*

Instructions:-

(i) The marks are indicated in the right-hand margin.

*(ii) There are **NINE** questions in this paper.*

*(iii) Attempt **FIVE** questions in all.*

*(iv) Question No. **1** is compulsory.*

Q.1 Choose the correct option of the following:(Answer any seven) **[2 x 7 = 14]**

(a) Dynamic RAM employs

(i) Capacitor or MOSFET (ii) FET or JFET

(iii) Capacitor or BJT (iv) BJT or MOS

(b) The resolution of a 10-bit AD converter for an input range of 10 V is approximately

(i) 1 V (ii) 1 mV (iii) 10 mV (iv) 100 mV

(c) The parameter through which 16 distinct values can be represented is known as

(i) bit (ii) byte (iii) word (iv) nibble

(d) If we record any music in any recorder, such type of process is called

(i) Multiplexing (ii) Encoding

(iii) Decoding (iv) Demultiplexing

(e) The systematic reduction of logic circuits is accomplished by

(i) Symbolic reduction (ii) TTL logic

(iii) Boolen algebra (iv) Truth table

(f) In which of the following base system, 123 is not a valid number?

(i) BASE 10 (ii) BASE 16 (iii) BASE 8 (iv) BASE 3

(g) A hexadecimal odometer displays F52F. The next reading will be

(i) F52E (ii) G52F (iii) F52F (iv) F530

(h) Sequential circuit contains;

(i) No memory element (ii) All input applied simultaneously

(iii) At least one memory element (iv) None

(i) How many entries will be in the truth table of a 4-input NAND gate.

(i) 6 (ii) 8 (iii) 32 (iv) 16

(j) Which ADC architecture is based on the principle of integrating an unknown input voltage over a fixed period of time?

(i) Flash ADC (ii) Successive Approximation ADC

(iii) Dual slope ADC (iv) Sigma-Delta ADC

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Q.2 (a) What are weighted, non-weighted, cyclic and self-complementary codes? Explain each with examples. [7]

(b) Find the values of X in the following conversions: [7]

(i) $(95 \cdot 10)_{10}$ to $(X)_2$

(ii) $(45 \cdot 70)_8$ to $(X)_2$

(iii) $(168 \cdot 16)_8$ to $(X)_{16}$

Q.3 (a) Design a BCD to 7-segment display decoder circuit using logic gates. [7]

(b) Design full adder using the following: [7]

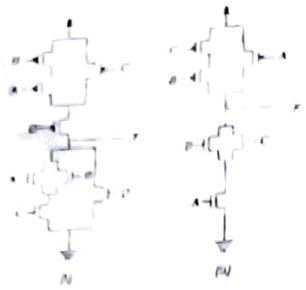
(i) 8:1 mux

(ii) 4:1 mux

Q.4 (a) Define resolution, linearity, accuracy and settling time of D/A converters. A typical D/A converter has a full-scale analog output of 10 v and accepts 6 binary bits as input. What will be the voltage corresponding to each analog step? [7]

(b) Design a 3-bit parallel comparator A/D convertor that provides output in 2's complement format. [7]

Q.5 (a) Identify the following logic functions implemented at F: [7]



(b) Implement the following CMOS logics: [7]

(i) $\overline{AB(A+B)}$

(ii) $\overline{((CD)+B)A}$

Q.6 (a) What is binary shift register? Write down their application. [7]

(b) Describe about Jhonson ring counter using four D-flip-flop. [7]

Q.7 (a) Minimize the following expression using k-map [7]

$f(P, Q, R, S) = \Sigma m(0,1,4,5,7,12,13)$

(b) Draw symbol and write the truth table of JK flip flop. [7]

Q.8 (a) Describe the procedure to design Mod-6 counter. [7]

(b) Explain SIPO and SISO operations of shift register with relevant logic diagrams and truth tables. [7]

Q.9 Write short notes of the following [3.5x4]

(i) RAM

(ii) ROM

(iii) CMOS logic

(iv) Operation of TTL logic circuit working as NAND Gate